Subcontract XAT-4-33624-01

"Development of a Wide Band Gap Cell for Thin Film Tandem Solar Cells"

6th Quarterly Report

to

National Renewable Energy Laboratory

from

Institute of Energy Conversion
University of Delaware

For period 2/6/05 – 5/5/05

Task 1: I-III-VI_2-based Solar Cells

Cu(InGa)$(SeS)_2$ Film Growth

We have previously found that the incorporation of the chalcogen species S and Se in co-evaporated Cu(InGa)$(SeS)_2$ films relative to the evaporated fluxes depends on whether the film composition is Cu-rich or Cu-poor [1]. Films with Cu/(In+Ga) > 1 have S/Se content greater than in the flux while those with Cu/(In+Ga) < 1 have lower S/Se than the flux.

In this report, single and bi-layer Cu(InGa)$(SeS)_2$ evaporation processes to deposit films with E_g > 1.5 eV are compared. The simple single-layer process uses constant fluxes of Cu, In, Ga, Se, and S over a 60 min deposition time. A series of runs were done to verify the reproducibility of the depositions and devices. The composition ratios, determined by EDS, of the Cu(InGa)$(SeS)_2$ layers were [Cu]/[In+Ga] ~ 0.8 – 0.9, [Ga]/[In+Ga] ~ 0.5 – 0.6, and [S]/[S+Se] ~ 0.3. The solar cell properties (without AR coating) are listed in Table I. The band gaps of the Cu(InGa)$(SeS)_2$ layers calculated from the composition ratios of [Ga]/[In+Ga] and [S]/[S+Se] are also shown in Table I. Efficiencies of more than 9 % were reproducibly obtained with V_{oc} > 0.8 V. The best efficiencies are comparable to the best cell previously produced using this process and bandgap, which was achieved using Cu(InGa)Se_2 films with no S [2]. Fill factors (FF > 70%) are higher than previously reported [2].

For the bi-layer evaporation process, a Cu-rich Cu(InGa)$(SeS)_2$ layer deposition for 45 min is followed by an In-Ga-S-Se layer deposition for 15 min to form a slightly Cu-poor Cu(InGa)$(SeS)_2$ layer. As with the single layer process, the substrate temperature is fixed

at 550°C for the entire deposition. Figure 1 shows grazing incidence x-ray diffraction (GIXRD) results of the (112) plane for a $Cu(InGa)(SeS)_2$ film prepared by the bi-layer process with composition measured by EDS of Cu/(In+Ga) = 0.8, Ga/(In+Ga) = 0.6, and S/(Se+S) = 0.5. The data shows two distinct peaks with the peak at higher 2θ more prominent at higher incident angle. This is consistent with a two-layer structure containing a Se-rich top layer and a S-rich bottom layer formed by the Cu-rich and then Cu-poor deposition. The distinct peaks indicate little interdiffusion between the separate compositions. Compositional depth profiles measured by AES will be used to characterize this layered structure and whether Ga/(In+Ga) is uniform through the film.

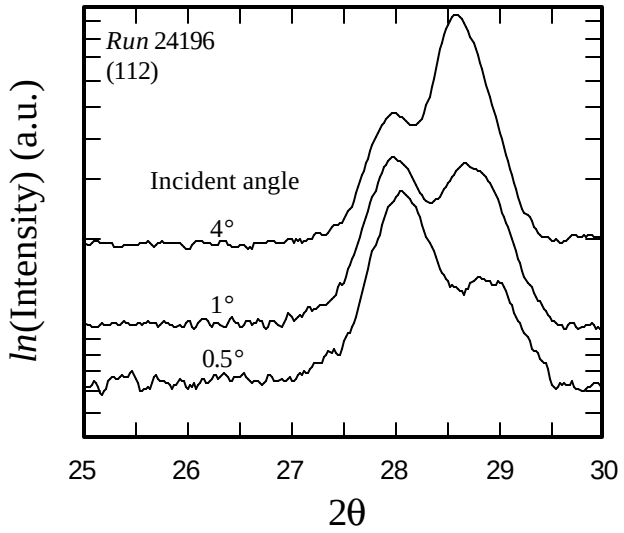

Figure 1. Typical GIXRD profiles from (112) plane of an as-deposited $Cu(InGa)(SeS)_2$ film prepared using the bi-layer process.

The properties of the bi-layer $Cu(InGa)(SeS)_2$ solar cells are listed in Table II. EDS measurements of the films gave Ga/(In+Ga) ~ 0.6 and S/(Se+S) ~ 0.3 – 0.8. E_g determined from the EDS composition is shown, although, in this case, it indicates an average bandgap due to the two-layer structure. The best cells, from run 24203 show 10 % efficiency, comparable to or better than the single-layer process. It is noteworthy that these cells have FF as high as 77%. The low efficiencies of the other devices in Table II are on cells having wider bandgap $Cu(InGa)(SeS)_2$ and lower J_{sc}.

Table I. J-V parameters for $Cu(InGa)(SeS)_2$ cells prepared using the single layer process. E_g is estimated from the EDS composition.

Run #	Eff. (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	E_g from EDS (eV)
24177	9.3	0.845	15.4	71.7	1.57
24185	8.8	0.822	17.1	62.8	1.50
24186	9.4	0.841	17.0	65.4	1.52
24188	9.6	0.817	16.8	69.7	1.53
24189	9.7	0.826	16.6	70.3	1.54
24190	10.0	0.822	17.1	70.9	1.55

Table II. J-V parameters for $Cu(InGa)(SeS)_2$ cells prepared using the bi-layer process.

Run #	Eff. (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	E_g from EDS (eV)
24195	6.7	0.847	11.7	68.1	1.72
24196	5.5	0.864	10.1	63.0	1.79
24197*	6.7	0.842	10.9	73.6	1.87
24198	4.7	0.836	11.0	51.2	1.79
24201	6.1	0.844	11.3	63.5	1.81
24203.1	10.5	0.802	17.0	76.7	1.62
24203.2	9.6	0.831	15.2	75.9	1.56

* KCN etched Cu rich sample

QE curves, measured under white light bias illumination, and J-V curves of cells from the run 24203 by the bi-layer process and from the run 24190 by the single layer process are shown in Figures 2 and 3 respectively. From the long wavelength QE edge, an effective band gap of the $Cu(InGa)(SeS)_2$ layers can be estimated. The single layer cell 24190 has $E_g \sim 1.55$ eV and for the bi-layer devices from 24203, it is similar or slightly greater. Further analysis to quantify the difference in these devices is underway.

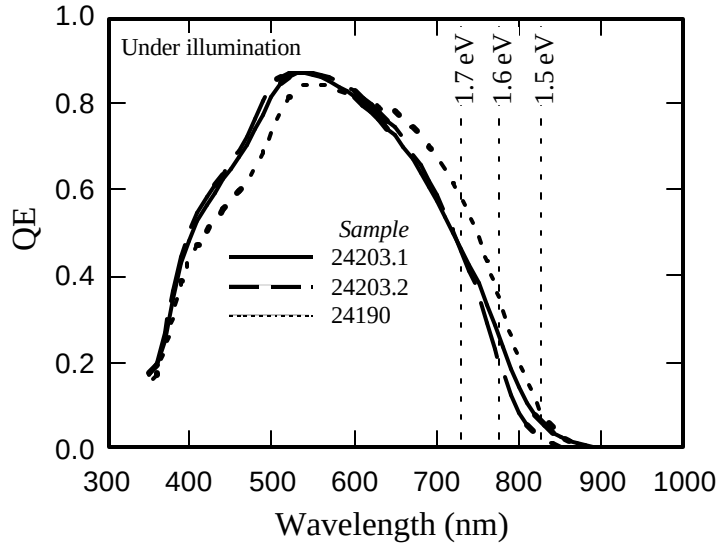

Figure 2. External QE of $Cu(InGa)(SeS)_2$ solar cells. Samples 24203 were deposited with a bi-layer process and 24190 with the single-layer process.

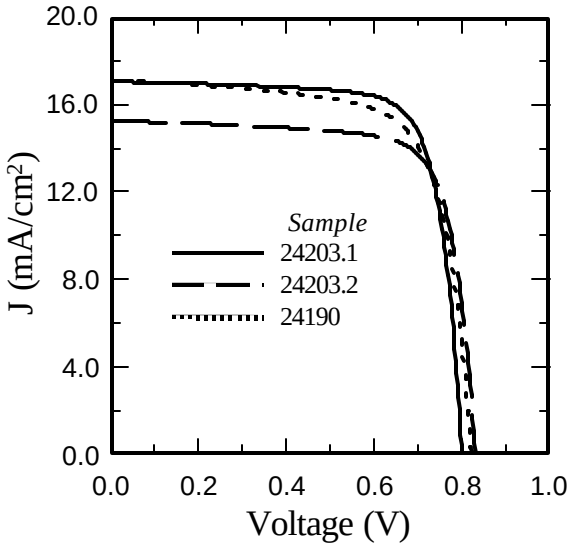

Figure 3. J-V curves of CIGSS solar cells. Samples 24203 were deposited with a bi-layer process and 24190 with the single-layer process.

$Cu(InGa)(SeS)_2$ Device Analysis

An over-riding problem preventing high efficiency in $Cu(InGa)(SeS)_2$ based solar cells with $E_g = 1.5$ eV is their low V_{OC}. The J-V behavior of a $Cu(InGa)(SeS)_2$ device can be described by a basic diode equation [3]

$$J = J_0 \exp\left[\frac{q}{AkT}(V - RJ)\right] + GV - J_L$$

with the diode current J_0 given by

$$J_0 = J_{00} \exp\left(\frac{\Phi_b}{AkT}\right).$$

The ideality factor A, barrier height Φ_b, and prefactor J_{00} will be dependent on the specific recombination mechanism that dominates the forward current J_0. Then, for $G << J_L/V_{OC}$, the open circuit voltage is:

$$V_{OC} = \frac{\Phi_b}{q} - AkT\, ln\left(\frac{J_{00}}{J_L}\right).$$

The barrier height Φ_b can be determined by measuring V_{OC} versus T and extrapolating to T = 0. We previously compared devices with Cu(InGa)Se_2, deposited with Cu/(In+Ga) < 1, and $CuInS_2$, deposited with Cu/(In+Ga) > 1 and then etched, which both have E_g = 1.5 eV [2]. The Cu(InGa)Se_2 cell had Φ_b = 1.5 eV and the $CuInS_2$ device had Φ_b = 1.1 eV. This is consistent with the Cu(InGa)Se_2 device having V_{OC} limited by space charge recombination, while the $CuInS_2$ device is limited by interface recombination. Thus, interface recombination may account for the lower V_{OC} with $CuInS_2$.

V_{OC}(T) is compared in Figure 4 for the devices in Table III, which have Cu(InGa)$(SeS)_2$, deposited with a single layer Cu-poor process. The cells with S have lower Φ_b ~ 1.2 eV. This suggests that the dominant recombination path in the S-containing devices may not be in the absorber layer, and interface recombination may account for the lower V_{OC}. In the next quarter, cells will be fabricated comparing CdZnS emitter layers to CdS to determine if the change in band alignment at the interface might reduce the recombination.

Table III. Barrier height Φ_b determined from V_{OC}(T) for devices with Cu(InGa)$(SeS)_2$ deposited by a single layer Cu-poor process with E_g = 1.5 eV.

sample	Ga / In+Ga	S / S+Se	E_g from EDS (eV)	V_{OC} (V)	Φ_b (eV)
24073	0.76	0	1.49	0.835	1.4
24074	0.60	0.26	1.53	0.861	1.2
24075	0.36	0.49	1.50	0.729	1.2
24077	0.23	0.68	1.52	0.669	1.3

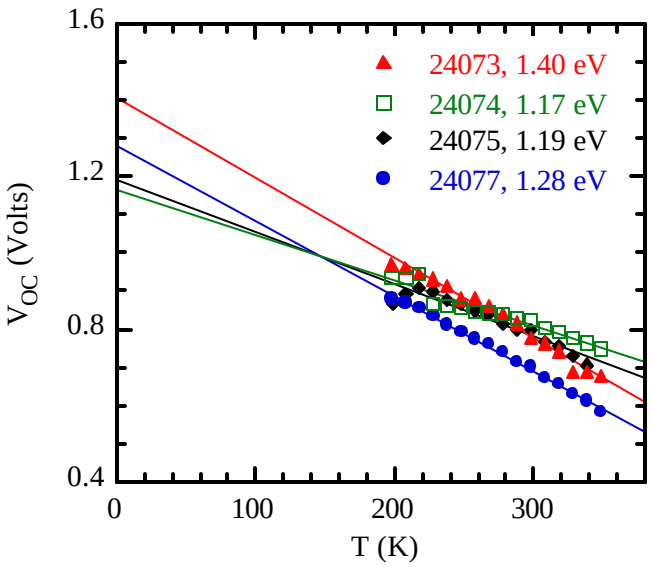

Figure 4. $V_{OC}(T)$ for cells with 1.5 eV $Cu(InGa)(SeS)_2$ deposited with a single layer Cu-poor process.

Task 2: II-VI- based Solar Cells

CdZnS Window Layers

Chemical surface deposited (CSD) $Cd_{1-x}Zn_xS$ films with x ~ 0.2 and E_g ~ 2.55 eV were incorporated as window layers in devices with $Cd_{1-x}Zn_xTe$ absorber layers. The purpose of incorporating Zn on the window side of the device is to reduce the driving force for Zn diffusion from the absorber side during the $ZnCl_2$ treatment of the device structure. This diffusion process results in phase segregation at the interface, which is correlated with low J_{sc} in devices. For superstrate cells, chemical surface deposition is preferred over chemical bath deposition due to the elimination of particulates arising from homogeneous bath nucleation. These particulates are relatively benign for substrate configuration cells but cause chemical non-uniformity in the interface region of superstrate cells during high temperature processing.

For the first set of samples, with $Cd_{1-x}Zn_xS$ deposited by CSD from a solution with Cd/Zn < 3 at 55ºC, yielding x ~ 0.2 and E_g ~ 2.55 eV, poor adhesion was obtained at the $Cd_{1-x}Zn_xS$-$Cd_{1-x}Zn_xTe$ interface after $ZnCl_2$ processing. GIXRD analysis of the films showed distinct phase segregation of Cd-rich and Zn-rich sulfide phases during both the 600ºC anneal step and the 415ºC $ZnCl_2$ treatment.

To achieve more definitive results with $Cd_{1-x}Zn_xS/Cd_{1-x}Zn_xTe$ structures, both the $Cd_{1-x}Zn_xS$ film growth process and film durability were characterized, in particular: 1) sensitivity of Zn incorporation to deposition temperature; 2) dependence of film composition on solution composition; and 3) chemical stability of the films during device processing steps. The deposition process used stock aqueous solutions of 0.015 M

$CdSO_4$, 0.15 M $ZnSO_4$, 1.5 M , thiourea, $CS(NH_2)_2$, and 14.28 M ammonium hydroxide. The required amounts of each solution and deionized water were mixed in a preparatory beaker, and the mixed solution was dispensed onto the substrate at the desired working temperature.

For a solution having a Zn/Cd ratio of 4, with [Zn] = 1.2 mM and [Cd] = 0.3 mM, Figure 5 shows that the growth rate was constant from 45ºC to 55ºC (15-20 Å/min) and increased by 3X at 65ºC (60 Å/min). The band gap, determined from plots of α^2 versus energy, decreased with increasing deposition temperature, from 2.82 eV at 45ºC (x = 0.45) to 2.58 eV at 65ºC (x = 0.22). The Zn in the solution thus limits the alloy reaction and is only weakly incorporated at higher temperatures, due in part to competing reactions, which form zinc hydroxides and zinc oxides. GIXRD measurements of films deposited at 45ºC and 55ºC were inconclusive due to a combination of low film thickness and poor crystallinity. However, the film deposited at 65ºC revealed a broad peak at d = 3.31Å , which corresponds to the (002) reflection of $Cd_{1-x}Zn_xS$ with x = 0.2, which is expected to yield an optical band gap of 2.55 eV. This is very close to the measured band gap.

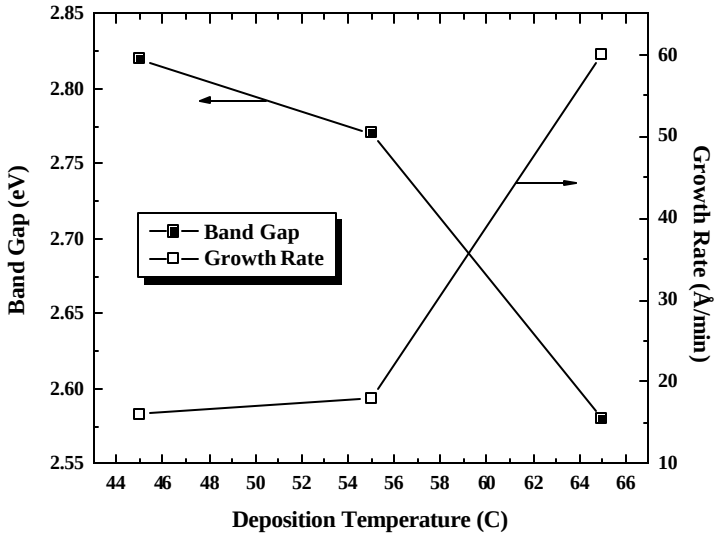

Figure 5. $Cd_{1-x}Zn_xS$ film band gap and deposition rate versus deposition temperature for solution with fixed composition: Zn:Cd = 4:1.

For depositions carried out at a fixed temperature (55ºC), the Zn/Cd ratio in the solution reduced the film growth rate from 130A/min at Zn/Cd = 0 to 20 Å/min at Zn/Cd = 4. However, increasing the ratio in the solution proportionally increased the band gap, from 2.4 eV (x = 0) at Zn/Cd = 0 to 2.8 eV (x = 0.45) at Zn/Cd = 4 (Figure 6). The growth of 300-500 nm thick films required for solar cell structures was accomplished by performing several consecutive depositions.

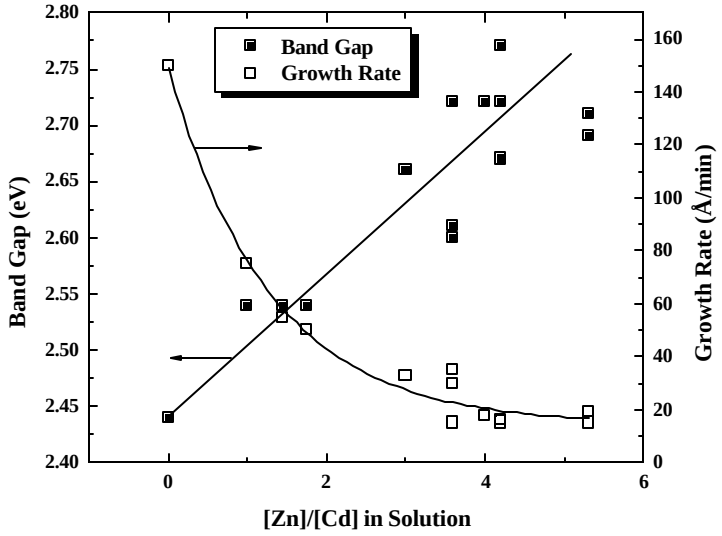

Figure 6. $Cd_{1-x}Zn_xS$ film band gap and deposition rate versus ratio of Zn/Cd ratio at 55ºC.

Some $Cd_{1-x}Zn_xS$ films deposited at 55ºC with Zn/Cd < 3 are unstable during subsequent annealing in air or in air plus $CdCl_2$ vapor. In these cases, the band gap reduces to near the value for pure CdS (2.44 eV) due to reaction of Zn with oxygen in the ambient. However, all the films deposited at higher Zn/Cd = 4 are stable, and there is no detectable change in band gap or phase content. These results are different than obtained for PVD $Cd_{1-x}Zn_xS$ films deposited at 200ºC, which are thermally and chemically stable over the entire range of Zn composition. The effect of deposition temperature on the stability is still under investigation.

CdZnTe Solar Cells

The vapor transport (VT) deposition procedure was modified to allow higher Zn content to be obtained in $Cd_{1-x}Zn_xTe$ films. Single phase $Cd_{1-x}Zn_xTe$ films with x up to 0.7 and E_g = 1.95 eV have been deposited at 550ºC onto 10 cm x 10 cm CdS/GaO/TEC-15 superstrates at ~ 5 µm/min. Plates from depositions spanning a range of Zn content were cut into 5 cm x 2.5 cm samples, and solar cells were completed with sequential processing: 600ºC anneal in argon for 15 minutes; $ZnCl_2$ vapor treatment in argon ambient at 415ºC for 15 minutes; etching in HCl followed by bromine in methanol; deposition of 8 Cu/Ni contacts with area 0.36 cm^2. The J-V parameters of the best devices for this series of films are shown in Table IV. The cells with low Zn content, at x = 0 and x = 0.05 serve as control samples for this set of data and have lower performance than cells from the same VT plates processed earlier in the year. It is believed that in spite of having stored the samples under vacuum and processing in minimal oxygen, exposure to ambient having relative humidity > 50%, may deteriorate the $Cd_{1-x}Zn_xTe$, even prior to $ZnCl_2$ processing. Although the overall experiment is plagued by these

concerns, the cells fabricated with higher Zn content, $0.1 < x < 0.6$, exhibit higher J_{sc} than had been previously obtained with PVD cells, fabricated in the previous phase of the contract. The V_{oc} shows no obvious trend with respect to Zn content, suggesting that the junction operation is dominated by another parameter. Cells from runs having $x = 0.8$ (VT156 and VT158) were electrically shorted and are not listed in the table.

Table IV. Performance of best cells obtained with $Cd_{1-x}Zn_xTe$ absorber layers.

Run	x	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
VT140.5	0	673	15.0	51	5.1
VT129.1	0.05	690	12.5	38	3.3
VT142.5	0.10	551	22.3	47	5.8
VT152.4	0.27	687	20.8	46	6.7
VT160.5	0.60	414	1.6	32	0.2

Superstrate and substrate configurations

Difficulties in processing cells with a superstrate configuration are primarily due to the strong chemical interaction between the window and absorber layers and the high reactivity of $Cd_{1-x}Zn_xTe$ films with ambient. An approach for overcoming this may be adoption of a *substrate* configuration. Although the substrate CdTe cell configuration has not yet demonstrated high performance, it may offer an approach for understanding junction formation and cell operation with $Cd_{1-x}Zn_xTe$ absorber layers. A single VT CdTe deposition with CdTe thickness of 5 µm was performed on a variety of substrates: Mo/SL glass, $MoTe_2$/Mo/SL glass, Cu_2Te/Mo/SL glass, and Cu_2Te/SnO_2/SL glass. Mo was deposited by sputtering. $MoTe_2$ films 200 nm thick were formed on the Mo films by reaction with Te + H_2 vapor at 400ºC for 1 minute. Cu_2Te films were deposited by co-evaporation of Cu and Te onto Mo-coated and SnO_2-coated SL glass substrates at 200ºC. Cells were fabricated by deposition of CdS by CBD, heat treatment with $CdCl_2$ + air at 420ºC for 20 minutes, and deposition of the same ZnO/ITO/Ni/Al structures used to process $Cu(InGa)(SeS)_2$ cells. The J-V parameters obtained for cells with opaque back contacts and 0.47 cm^2 area are listed in Table V. In the table, promising J_{sc} values are shown for cells made with Cu_2Te and $MoTe_2$ contacts, while extremely low junction performance is obtained with a bare Mo substrate.

Table V. Performance of opaque CdTe/CdS cells in substrate configuration.

Run	Contact	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
VT171.11	Mo	90	0.2	-	-
VT171.43	$MoTe_2$/Mo	288	15.3	26	1.1
VT171.31	Cu_2Te/Mo	343	14.5	36	1.8

GIXRD measurements of the CdS-CdTe interface region after the $CdCl_2$ region showed a preponderance of $CdTeO_3$ reflections but none due to $CdSO_4$. Future cells will receive $CdCl_2$ treatment at reduced oxygen partial pressure.

Transparent cells

We have fabricated CdTe/CdS solar cells with >50% sub band gap transmission in superstrate configuration and ~30% sub band gap transmission in substrate configuration, using vapor transport deposition for the CdTe film. The superstrate cells utilized CdTe films with thickness from 0.5 to 7 μm. Cells made with CdTe thickness less than 1.5 μm were shorted. The J-V parameters for the other cells are listed in Table VI. The optical transmission, T/(1-R), from 400 to 1400 nm for cells with 0.5, 1.5 and 7 μm thick CdTe are shown in Figure 7. In the superstrate mode, the cells were completed after $CdCl_2$ treatment by the BDH etch process, followed by evaporation of 2 nm Cu layer, sputter deposition of 200 nm ITO and evaporation of a Ni/Al grid with area 0.47 cm^2. In superstrate configuration, nearly 12% efficiency was obtained for a cell with 7 μm thick CdTe. The cell results for the thinner CdTe are unresolved, since >11% efficiency was obtained for cells on the same plate using Cu/Ni contacts.

Table VI. Performance of transparent CdTe cells in superstrate and substrate configurations.

Run	Configuration	CdTe Thk (μm)	V_{oc} (mV)	J_{sc} mA/cm^2	FF (%)	Eff (%)
VT174.2	Superstrate	7.0	790	23.5	64	11.8
VT153.2	Superstrate	1.5	454	19.8	35	3.2
VT171.41	Substrate	5.0	639	17.2	38	4.2

The transparent cell in substrate configuration, with 60 nm thick Cu_2Te back contact, has higher performance than its counterparts with opaque contacts listed in Table VI. However, the sub band gap optical transmission is only 30%.

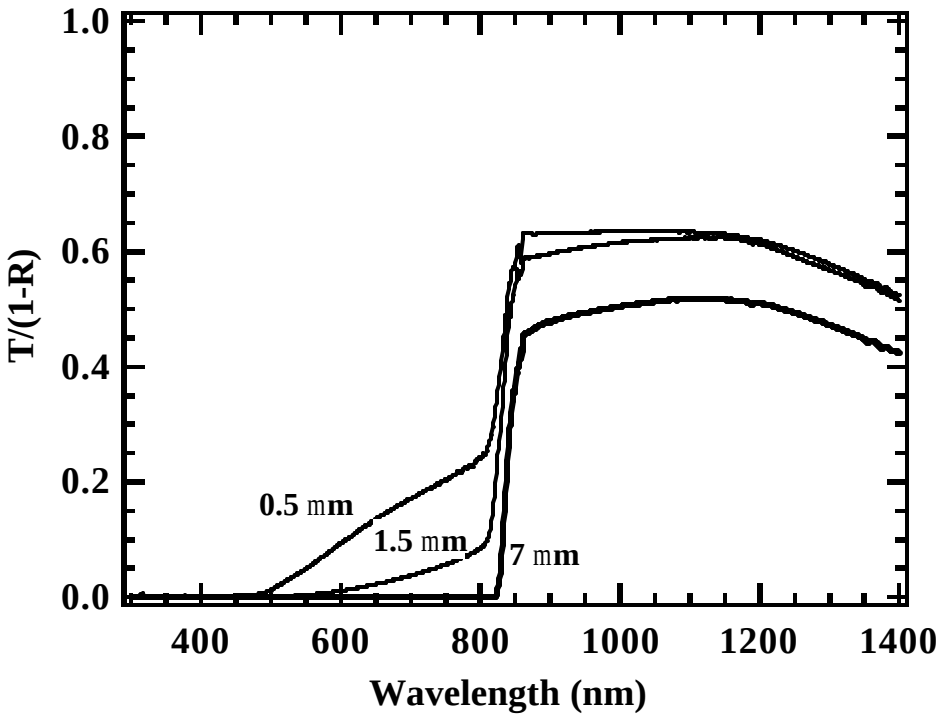

Figure 7. T/(1-R) of VT CdTe/CdS cells with different thickness CdTe films.

Collaboration

Collaboration is underway with the University of Toledo on development of cells with $Cd_{1-x}Mn_xTe$ absorber layers. $MnCl_2$ depositions followed by thermal treatments at 380ºC were carried out on the samples, which were returned to the University of Toledo for device fabrication.

References

1. A. Stavrides, C. Yapp, W. Shafarman, R. Aparicio, R. Opila, and R. Birkmire, Proc. 31st IEEE PVSC, 247 (2005).
2. W. Shafarman and P. Paulson, Proc. 31st IEEE PVSC, 231 (2005).
3. S.S. Hegedus, W.N. Shafarman, *Progress in Photovoltaics* **12**, 155 (2004).